10W Stereo Class D Audio Power Amplifier

BA3101

Data Sheet

Rev.1.0, 2009.08.01

Biforst Technology Inc.

10W Stereo Class D Audio Power Amplifier

GENERAL DESCRIPTION

The BA3101 is a 12V class D amplifier from Biforst Technology. BA3101 provide volume control with four selectable gain settings. BA3101 is a 10-W (per channel) with lower supply current and fewer external components for driving bridged-tied stereo speaker directly.

BA3101 operates with high efficiency energy conversion up to 89% (8-Ω Load) so that the external heat sink can be eliminated while playing music. Two gain select pins, GAIN0 and GAIN1, control the two controllable gain values, with firm gain selections are 20dB, 26dB, 32dB, 36dB.

BA3101 also integrates Anti-Pop, Output Short & Over-Heat Protection Circuitry to ensure device reliability. This device output are completely protected from shorts to ground or supply pin as well as protected from Output Pin to Output Pin short. All the output short protection features are auto restore and auto monitor.

FEATURE

- 9.2W Per Channel Into 8-Ω Speakers (THD+N = 10%@12V)
- 10.8W Per Channel into 8-Ω Speakers (THD+N = 10%@13V)
- Operation Voltage From 8V To 15V
- Maximum Power Efficiency Into 8-Ω, 89%
- Total four selectable, firm-gain solution
- Differential input
- Automatic monitor and restore scheme for short and over heat protection
- Clock synchronization master/slave for multiple Class D device
- Eliminates output clamp and bypass capacitors
- Package is SMD 7mm * 7mm 48 Pins TQFP-with Exposed Thermal Pad

APPLICATION

- LCD TV
- LCD Monitor
- Powered Speaker
- Hi-Fi Audio System

These devices have limited built-in ESD protection. The lead should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the device.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise specified (* 1)

SYMBOL	PARAMETER	VALUE	UNIT
VDD, PVDDL, PVDDR	Supply voltage	-0.3 to 15	V
V_I($\overline{\text{SHUTDOWN}}$, MUTE)	Input voltage	-0.3 to VCC+0.3	V
V_I(GAIN0, GAIN1, RINN, RINP, LINN, LINP, MSTR/ $\overline{\text{SLV}}$, SYNC)	Input voltage	-0.3 to VREG+0.5	V
T_A	Operating free-air temperature range	-40 ~ +85	°C
T_J	Operating junction temperature range(* 2)	-40 to +150	°C
T_{STG}	Storage temperature range	-65 to 85	°C
$R_{(Load)}$	Minimum load resistance	8	Ω
Electrostatic discharge	Human body model	±2	kV
Electrostatic discharge	Machine model	±200	V

(*1): Stress beyond those listed at “absolute maximum rating” table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up “recommended operation conditions” table.

(*2): BA3101 package embedded with an exposed thermal PAD underside of package. The exposed PAD performs the function of heat sink and it have to be connected to a thermally dissipating plane for power dissipation. Failure to do so will result in the device going into thermal protection shutdown.

PACKAGE DISSPATION RATINGS

PACKAGE	θja(junction to ambient air)	θjc(junction to case)	UNIT
TQFP 48 pin with Expose Pad	35.24	7.14	mW/℃

*This data was taken using 1 oz copper pad that is soldered directly to FR-4 PCB. The thermal pad must be soldered to the thermal land on PCB.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITION	SPECIFICATION		UNIT
			MIN	MAX	
V_{DD}	Supply voltage	VDD，PVDDL，PVDDR	8	15	V

SYMBOL	PARAMETER	TEST CONDITION	SPECIFICATION		UNIT
			MIN	MAX	
V_{IH}	High level input voltage	$\overline{SHUTDOWN}$ ，MSTR/ $\overline{SLV}$ ，SYNC，GAIN0，GAIN1，MUTE	2.0		V
V_{IL}	Low level input voltage	$\overline{SHUTDOWN}$ ，MSTR/ $\overline{SLV}$ ，SYNC MUTE，GAIN0，GAIN1		0.8	V
I_{IH}	High level input current	$V_I=V_{DD}$，V_{DD}=15 V		150	uA
		MUTE，$V_I=V_{DD}$，V_{DD}=15 V		80	
		$V_I=V_{REG}$，V_{DD}=15 V		2	
I_{IL}	Low level input current	$V_I=V_{DD}$，V_{DD}=15 V		2	uA
		V_I=0 V，V_{DD}=12 V		1	
V_{OH}	High level output voltage	FAULT，I_{OH}=1 mA，	V_{REG}-0.6		V
V_{OL}	Low level output voltage	FAULT，I_{OL}=-1 mA，		A_{GND} +0.4	V
f_{OSC}	Oscillator frequency	R_{OSC} Resistor = 100 kΩ，MSTR/ $\overline{SLV}$ = 2 V	250	300	kHZ
T_A	Operating free-air temperature		- 40	85	°C

DC CHARACTERISTICS

TA = 25℃, VDD= 12V, RL = 8Ω, Gain =20dB (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION		SPECIFICATION			UNIT
				MIN	TYP	MAX	
V_{REG}	5V internal supply voltage	No load		4.5	5	5.5	V
V_{BYP}	Bypass reference for input amplifier	No load		1.15	1.25	1.35	V
|PSRR|	DC power supply rejection ratio	V_{DD}=12V, input AC tie ground, Gain=36dB			70		dB
$R_{DS(ON)}$	Drain-Source on –state resistance	V_{DD}=12V, P_O=8W, R_L=8Ω	High Side		365		mΩ
			Low Side		365		
G	Gain	GAIN0=L	GAIN1=L		20		dB
			GAIN1=H		26		
		GAIN0=H	GAIN1=L		32		
			GAIN1=H		36		

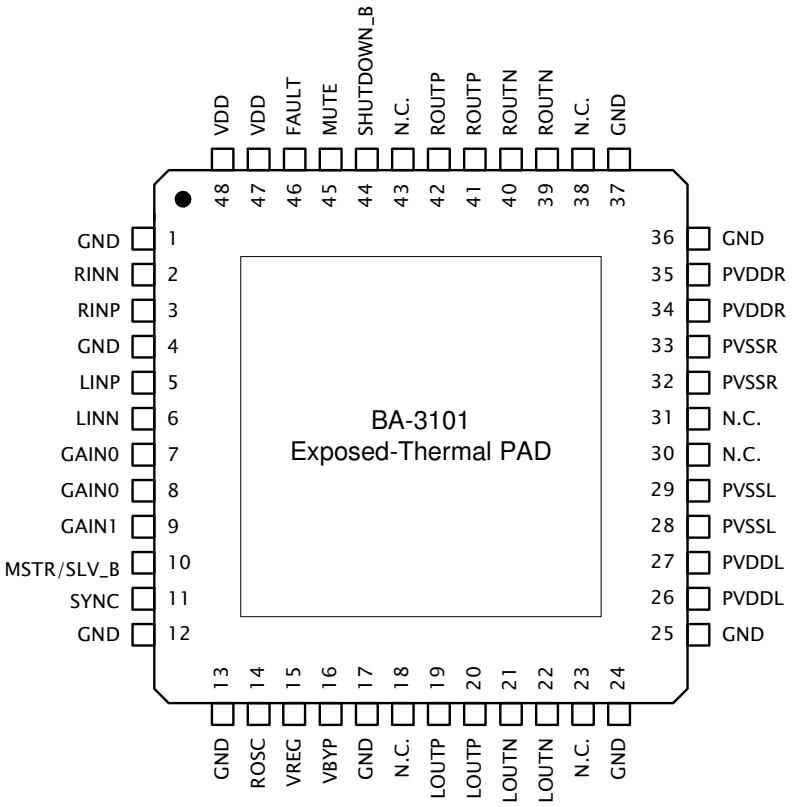
SYMBOL	PARAMETER	TEST CONDITION	SPECIFICATION			UNIT
			MIN	TYP	MAX	
T_{ON}	Turn-On time	C(V_{BYP})=1μF, $\overline{SHUTDOWN}$ =H		25		ms
T_{OFF}	Turn-Off time	C(V_{BYP})=1μF, $\overline{SHUTDOWN}$ =L		0.1		ms
I_{CC}	Quiescent	$\overline{SHUTDOWN}$ =H, MUTE=L, no load, no filter, no snubber		24		mA
	Mute mode	$\overline{SHUTDOWN}$ =H, MUTE=H, no load, no filter, no snubber		11		
	Shutdown mode	$\overline{SHUTDOWN}$ =L, no load, no filter, no snubber		200μA		

AC CHARACTERISTICS

TA = 25℃, VDD= 12V, RL = 8Ω, Gain =20dB (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION		SPECIFICATION			UNIT
				MIN	TYP	MAX	
|Ksvr|	Supply ripple rejection	200mV_{PP} ripple from 20Hz-1kHz, input AC tie ground			70		dB
THD+N	Total harmonic distortion and noise	f=1kHz, P_O=5W			0.17		%
|Crosstalk|	Crosstalk between L/R channel	Vo=1V_{RMS},f=1kHz			90		dB
P_O	Continuous output power	f=1kHz	THD+N=1%		7.4		W
			THD+N=10%		9.2		
			V_{DD}=13V,THD+N=10%		10.8		
SNR	Signal to noise ratio	THD+N=1%, A-weighted, f=1kHz			93		dB
V_N	Output noise	22Hz to 22kHz, A-weighted filter			150		μV

PIN ASSIGNMENTS

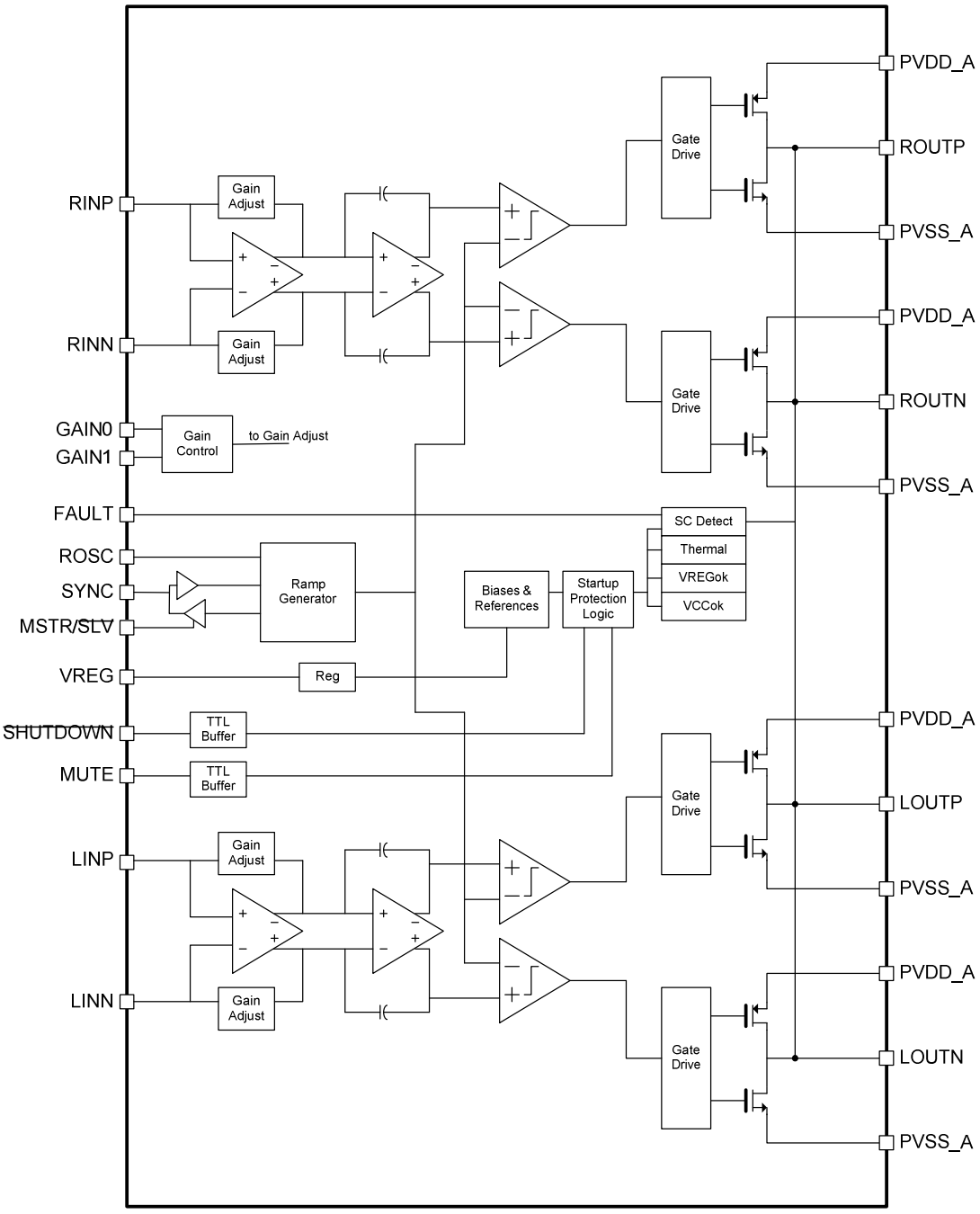


PIN DESCRIPTION

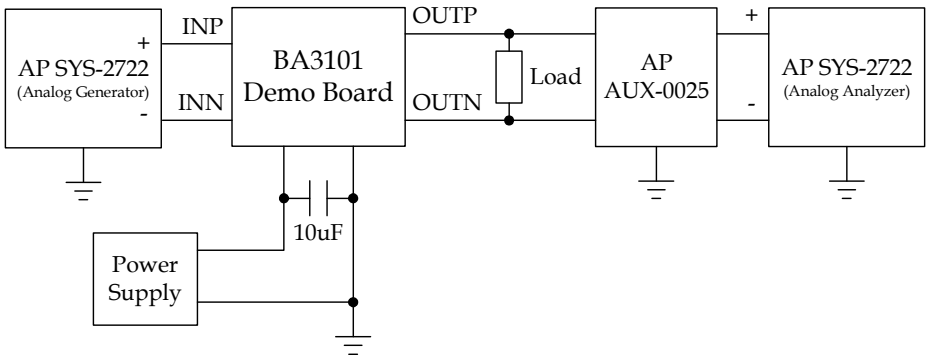
Pin No.	Pin	Type	I/O Pad Function
1	GND	POWER	Power ground
2	RINN	Input	Right channel negative audio signal input
3	RINP	Input	Right channel positive audio signal input
4	GND	POWER	Power ground
5	LINP	Input	Left channel positive audio signal input
6	LINN	Power	Left channel negative audio signal input
7 ~ 8	GAIN0	Input	Gain control input to select least significant bit
9	GAIN1	Input	Gain control input to select most significant bit
10	MSTR/ $\overline{\text{SLV}}$	Input	Determine clock operating mode. While this pin is H state, BA3101 operates in clock master mode, SYNC outputs operating clock, otherwise the operating mode is clock Slave mode, SYNC pin accept clock input.
11	SYNC	Input/Output	Could be input or output clock to synchronize multiple class D devices. I/O direction is decided by "MSTR/ $\overline{\text{SLV}}$ " pin.
12 ~ 13	GND	Power	Power ground
14	ROSC	Input/Output	External resistor for current control
15	VREG	Output	5V voltage regulation output for internal reference.
16	VBYP	Output	Bias reference voltage output, need connect an external capacitor.
17	GND	Power	Power ground
18	NC		

19 ~ 20	LOUTP	Output	Left channel positive output
21 ~ 22	LOUTN	Output	Left channel negative output
23	NC		
24 ~ 25	GND	Power	Power ground
26 ~ 27	PVDDL	Power	Power supply for left channel output
28 ~ 29	PVSSL	Power	Power ground for left channel output
30 ~ 31	NC		
32 ~ 33	PVSSR	Power	Power ground for right channel output
34 ~ 35	PVDDR	Power	Power supply for right channel output
36 ~ 37	GND	Power	Power ground
38	NC		
39 ~ 40	ROUTN	Output	Right channel negative output
41 ~ 42	ROUTP	Output	Right channel negative output
43	NC		
44	SHUTDOWN_B	Input	Shutdown signal for IC (L state = disabled, H state= normal). TTL logic levels with compliance to V_{DD}.
45	MUTE	Input	Signal to instantly disable output; Signal is TTL logic level compatible and compliance with V_{DD}.
46	FAULT	Output	Fault status indicator. HIGH = short-circuit fault. LOW = fault-free. Only reports short-circuit faults.
47 ~ 48	VDD	Power	Power supply.
	Exposed Thermal PAD		The thermal pad have to be soldered and be connect to the PCB large ground copper area.

FUNCTIONAL BLOCK DIAGRAM



TEST SETUP FOR PERFORMANCE MEASUREMENTS



Note: This connection diagram shows single channel configuration. All graphs were measured by BA3101 demo board. Two 22μH inductors are used in series with load resistor to emulate the speaker for efficiency measurement.

TYPICAL CHARACTERISTICS

Table of Graphs

Figure No.	Description	
1	THD+N vs. Output Power	Gain=20dB,Load=8Ω,VDD=12V
2	THD+N vs. Output Frequency	Gain=20dB,Load=8Ω,VDD=12V
3	Crosstalk vs. Frequency	Gain=20dB,Load=8Ω,VDD=12V, THD+N=1%
4	Gain and Phase	Gain=32dB,Load=8Ω,VDD=12V, C_{IN}=10μF,V_{IN}=0.1V
5	Output Power vs. Supply Voltage	Gain=20dB,Load=8Ω
6	Output Power vs. Current	Gain=32dB,Load=8Ω
7	Efficiency	Gain=32dB,Load=8Ω,VDD=12V

Important notice: Power above 10 W may require increased heatsinking.

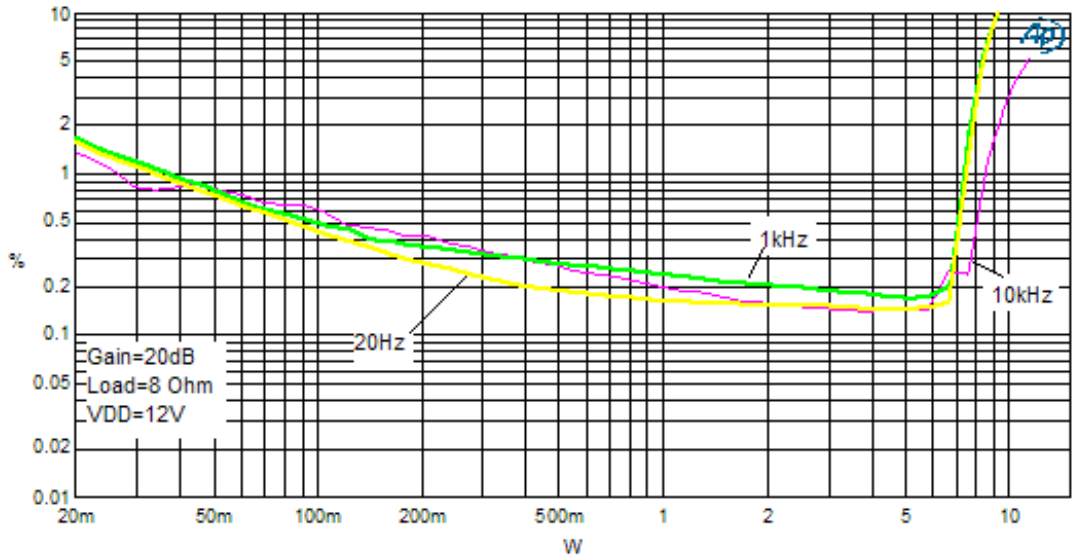


Figure 1. THD+N vs Output Power

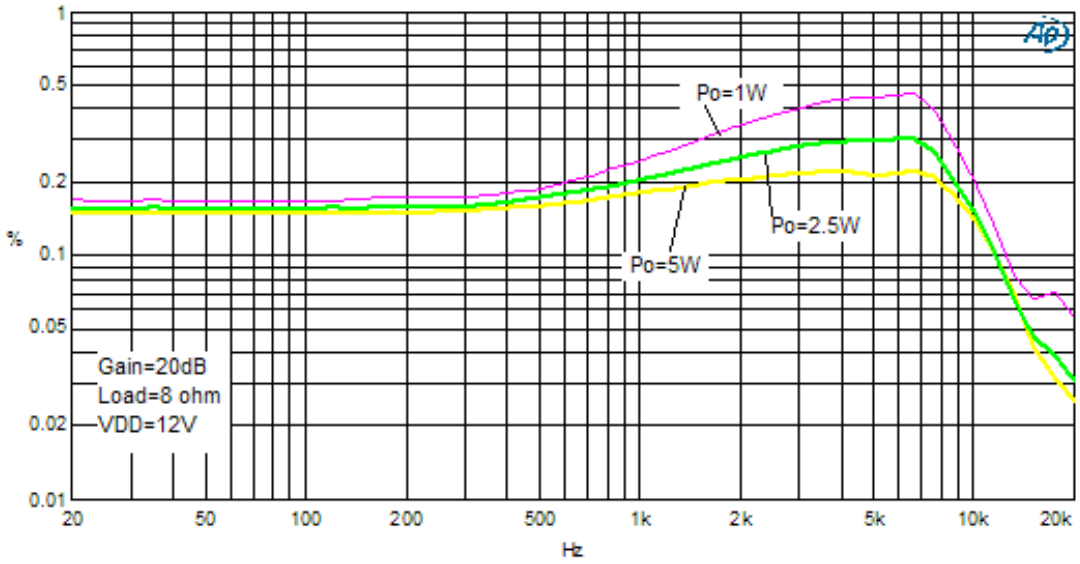


Figure 2. THD+N vs Frequency

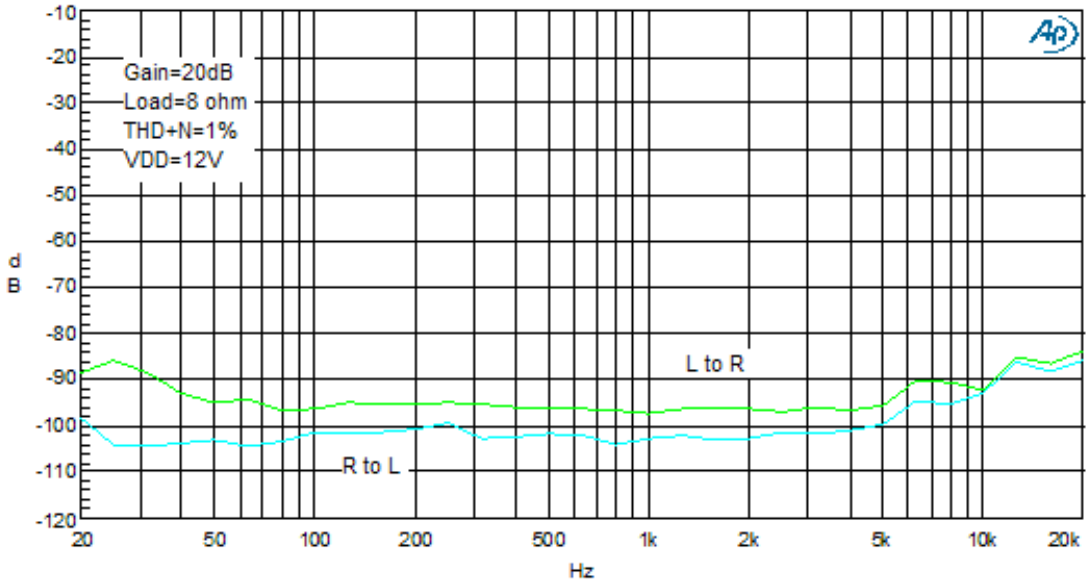


Figure 3. Crosstalk vs Frequency

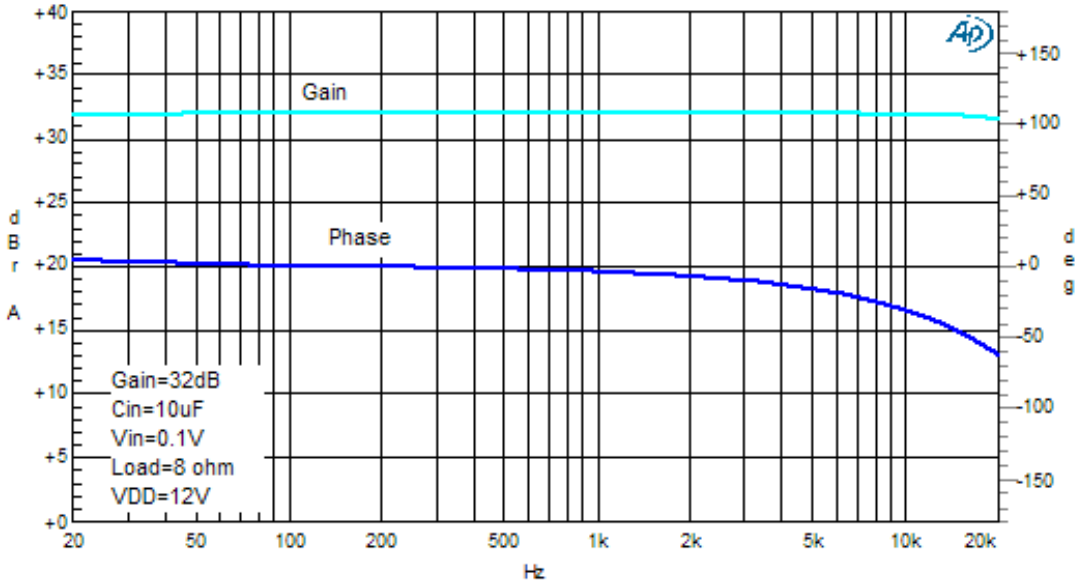


Figure 4. Gain and Phase Shift vs Frequency

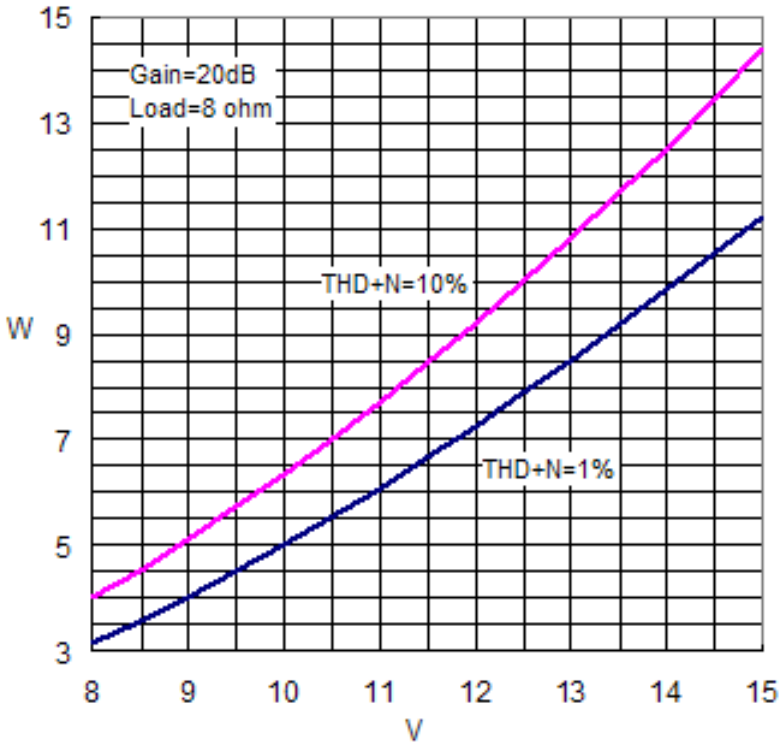


Figure 5. Output Power vs Supply

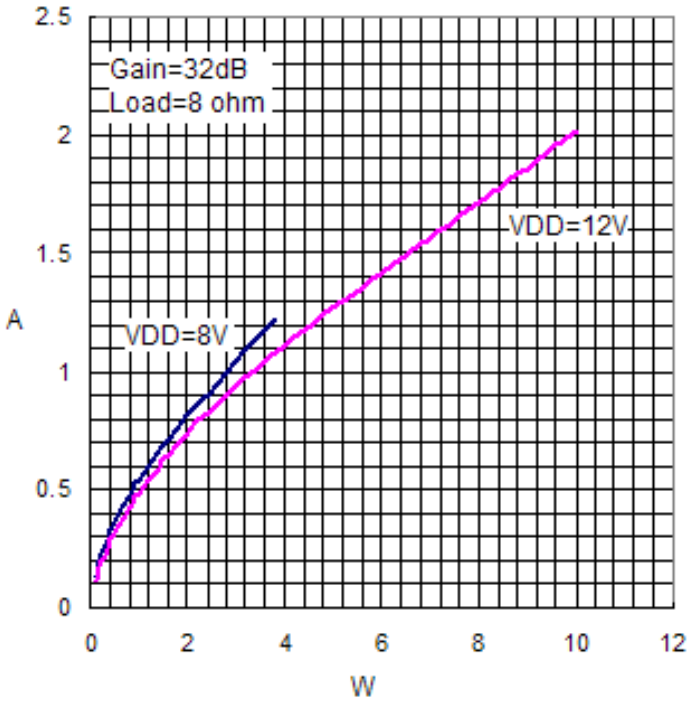


Figure 6. Supply Current vs Output Power

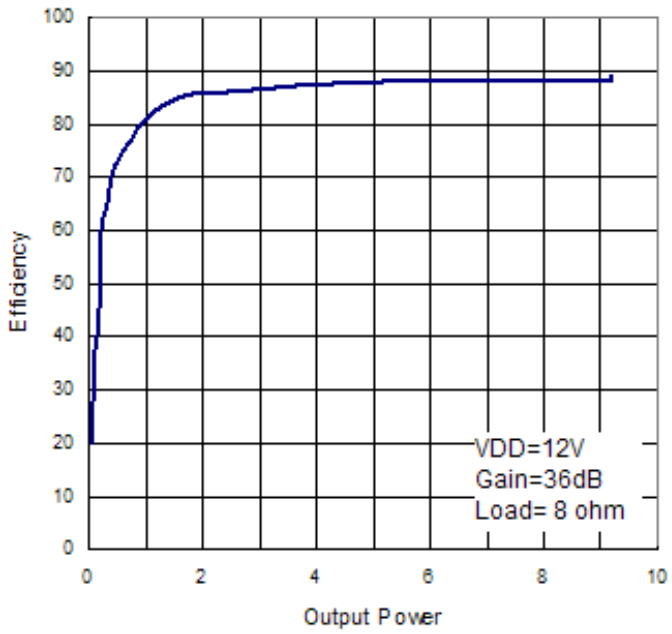


Figure 7. Efficiency

FUNCTION DESCRIPTION

Output Filter Application Note

Design the BA3101 without the filter if the traces from amplifier to speaker are short (< 10cm), where the speaker is in the same enclosure as the amplifier is a typical application for class D without a filter. Many applications require a ferrite bead filter. The ferrite filter reduces EMI around 30MHz. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and there are long wires from the amplifier to the speaker.

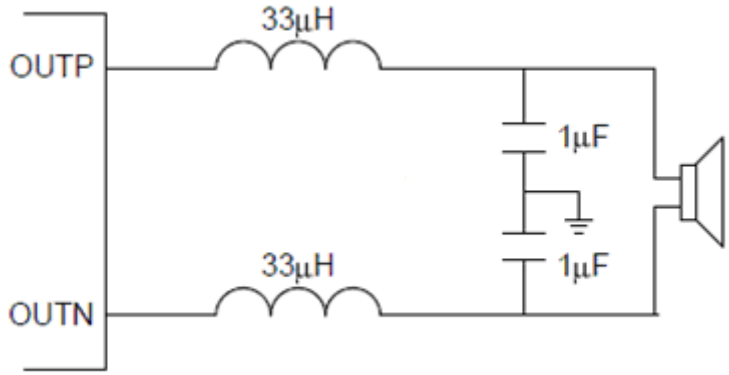


Figure 8. Typical LC Output Filter, Speaker Impedance=8Ω

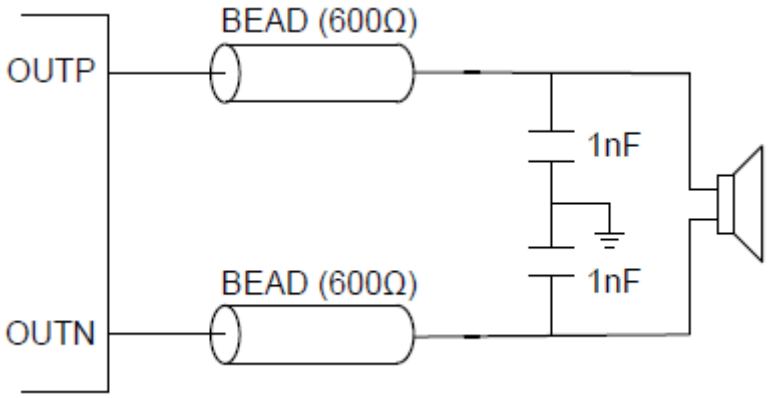


Figure 9. Typical Ferrite Chip Bead Output Filter, Speaker Impedance=8Ω

Inductors used in LC filters must be selected carefully. A significant change in inductance at the peak output current of the BA3101 will cause increased distortion. The change of inductance at currents up to the peak output current must be less than 0.1µH per amp to avoid this. Also note that smaller inductors than 33µH may cause an increase in distortion above what is shown in preceding graphs of THD versus frequency and output power. In all cases, avoid using inductors which value are less than 22µH.

Capacitors used in LC filters must also be selected carefully. A significant change in capacitance at the peak output voltage of the BA3101 will cause increased distortion. LC filter capacitors should have DC voltage ratings of at least twice the peak application voltage (the power supply voltage). In all cases, it is strongly recommended using capacitors with good temperature ratings like X5R.

Output Snubbers

In Figure 11, the 470pF capacitors in series with 22Ω resistors from the outputs of the BA3101 to switching snubbers. They smooth switching transitions and reduce overshoot and ringing. By doing so they improve THD+N at lower power levels and they improve EMC by 2 to 4 dB at middle frequencies.

They increase quiescent current by 3mA to 11mA depending on power supply voltage.

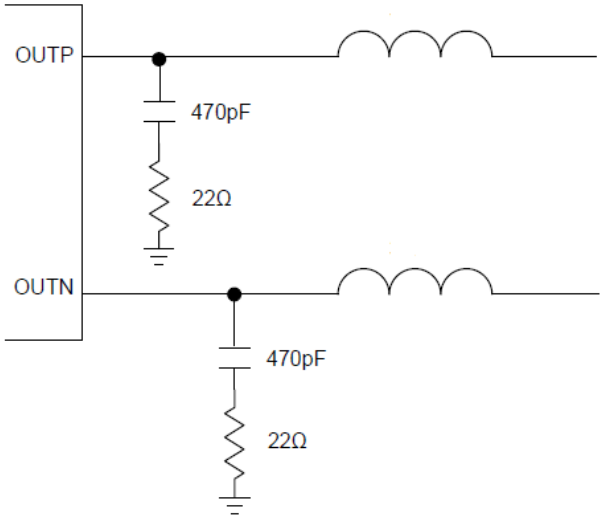


Figure 10. Output Snubbers

Over-Heat Protection

Over-Heat protection on the BA3101 prevents damage to the device when the internal die junction temperature exceeds 150℃. Once the die temperature exceeds the thermal set point, the device enters the shutdown state and the outputs are disabled. The device will back to normal operation when die temperature is reduced without external system interaction.

Output Short Protection

The BA3101 has output short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output short, output-to-GND short and output-to-VDD short. BA3101 enter the shutdown state and the outputs are disabled when detects output short. This is a latched fault and must be reset by cycling the voltage on $\overline{\text{SHUTDOWN}}$ pin or MUTE pin, or by cycling the power off and then back on. This clears the short circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry would active again.

Internal 5V reference

The VREG terminal (pin 15) is the output of an internally generated 5V supply, used for the oscillator, preamplifier, and gain control circuitry. It is highly recommended to place a 10nF~100nF capacitor close to the pin to keep the internal regulator stable. This regulated voltage should be used to connect GAIN0, GAIN1, MSTR/ $\overline{\text{SLV}}$, and MUTE terminals only. Do not use it to drive external circuitry.

Bypass Capacitor

The internal bias generator (V_{BYP}) nominally provides a 1.25V bias for the preamplifier stages using internally. The input coupling capacitors and this internal voltage reference allow the inputs to be biased

within the optimal common-mode range of the input preamplifiers. The value of the capacitor on the V_{BYP} terminal (pin 16) is critical related to amplifier performance. During power up or recovery from the shutdown state, this capacitor determines the rate at which the amplifier starts up. Using a larger value of V_{BYP} capacitor can increase amplifier start-up time but should not exceed 10µF.

Selection of R_{OSC}

The class D output switching frequency can be controlled by R_{OSC} and C_{OSC} by the following equation:

$$f_{OUT} = \frac{1}{2 \times R_{OSC} \times C_{OSC}}$$

R_{OSC} is an external resistance connected to pin 14 that is nominally 100kΩ. C_{OSC} is an internal capacitor that is nominally equal to 18 pF. Variation over fabrication process and temperature can result in a ±15% change in this capacitor value. For example, if R_{OSC} is fixed at 100kΩ, the frequency from device to device with this fixed resistance could vary from 300 kHz to 250 kHz including the variations of R_{OSC} resistor.

LOW-ESR Capacitors

Low-ESR capacitors are high recommended for this application. Generally a practical capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this unwanted resistor can eliminate the effects of the ideal capacitor. Place low ESR capacitors on supply circuitry can improve THD+N performance.

Decoupling Capacitors

BA3101 requires appropriate power decoupling to minimize the output total harmonic distortion (THD). Power supply decoupling also prevents intrinsic oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply lines. For higher frequency spikes, or digital hash on the rail, a good low ESR ceramic capacitor, for example 0.1µF to 10µF, placed as close as possible to PVDD_A pins works best. For filtering lower frequency noise, a larger low ESR aluminum electrolytic capacitor of 220µF or greater placed near the audio power amplifier is also recommended. The 220µF capacitor also serves as local storage capacitor for supplying current during heavy duty on the amplifier outputs. The PVDD_A terminals provide the power to the output transistors, so a 220µF or larger capacitor should be placed on each channel PVDD_A terminal. A 10µF ceramic capacitor on each VDD terminal is also recommended.

Gain Settings

The gain of the BA3101 can be set by GAIN0 and GAIN1 pins. The gain ratios listed in Table are implemented by changing the taps on the feedback resistors in the preamplifier stage. Since the gain settings are controlled by ratios of input resistor and feedback resistor of the preamplifier, the gain ratio may varies with different V_{DD} supply. Note the amplifier gain ratio is obtained at 12V V_{DD} supply.

Gain 1	Gain 0	Gain Ratio
1	1	36dB
1	0	32dB
0	1	26dB
0	0	20dB

Table 1. BA3101 Gain Ratio

Differential Input

The differential input stage of the amplifier can cancel any common-mode noise coupled from input paths. To use the BA3101 with a differential signal source, connect the positive output of the audio source to the INP input and the negative output from the audio source to the INN input. To use the BA3101 with a single-ended signal source, ac ground the INP or INN input through a coupling capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In single-ended input configuration, the unused inputs should be ac grounded at the audio source instead of at the IC input for better noise performance.

$\overline{\text{SHUTDOWN}}$ OPERATION

The BA3101 employs a shutdown mode of operation designed to reduce supply current to the absolute minimum level during periods of nonuse for power conservation. This terminal should be held high during normal operation when the amplifier is in normal operating. Pulling low causes the output drivers shutdown and the amplifier to enter a low-current state. Do not leave it unconnected, because there is no weakly pulling resistor inside the amplifier. Remember that to place the amplifier in the shutdown state prior to removing the power supply voltage so that power-off pop noise can be eliminated.

MSTR/ $\overline{\text{SLV}}$ and SYNC Operation

The MSTR/ $\overline{\text{SLV}}$ and SYNC terminals can be used to synchronize the frequency of the class D output switching. When the MSTR/ $\overline{\text{SLV}}$ terminal is high, the output switching frequency is determined by the selection of the resistor connected to the ROSC terminal. The SYNC terminal becomes an output in this mode, and the frequency of this output is also determined by the selection of the ROSC resistor. This TTL compatible, push-pull output can be connected to another BA3101, configured in the slave mode. The output switching is synchronized to avoid any beat frequencies that could occur in the audio band when two class D amplifiers in the same system produces switching noises on V_{DD} supply. When MSTR/ $\overline{\text{SLV}}$ terminal is in low state, the output switching frequency is determined by the incoming square wave on the SYNC input. The SYNC terminal becomes an input in this mode and accepts a TTL compatible square wave from another BA3101 configured in the master mode or from an external GPIO. If connecting to an external GPIO, recommended frequencies are 225 kHz to 325 kHz for proper device

operation.

SAMPLE APPLICATION CIRCUIT

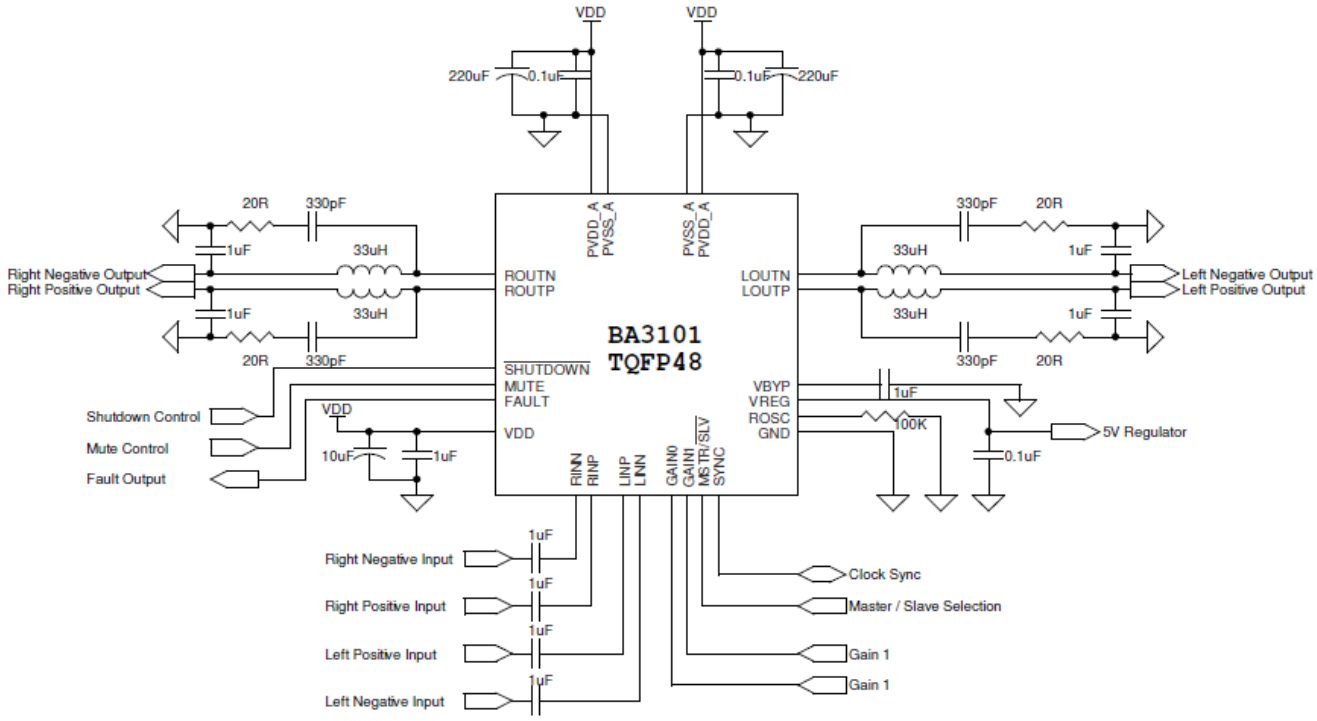


Figure 11. Stereo Class D with Differential Inputs

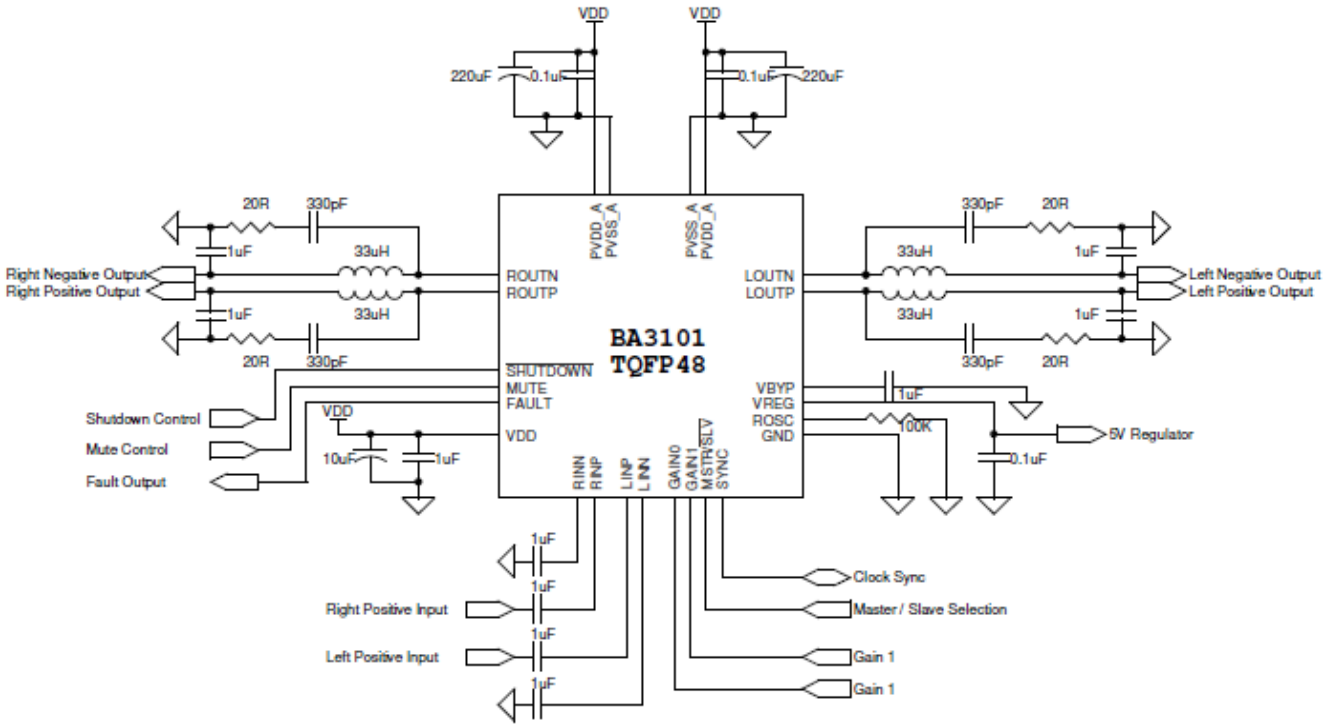
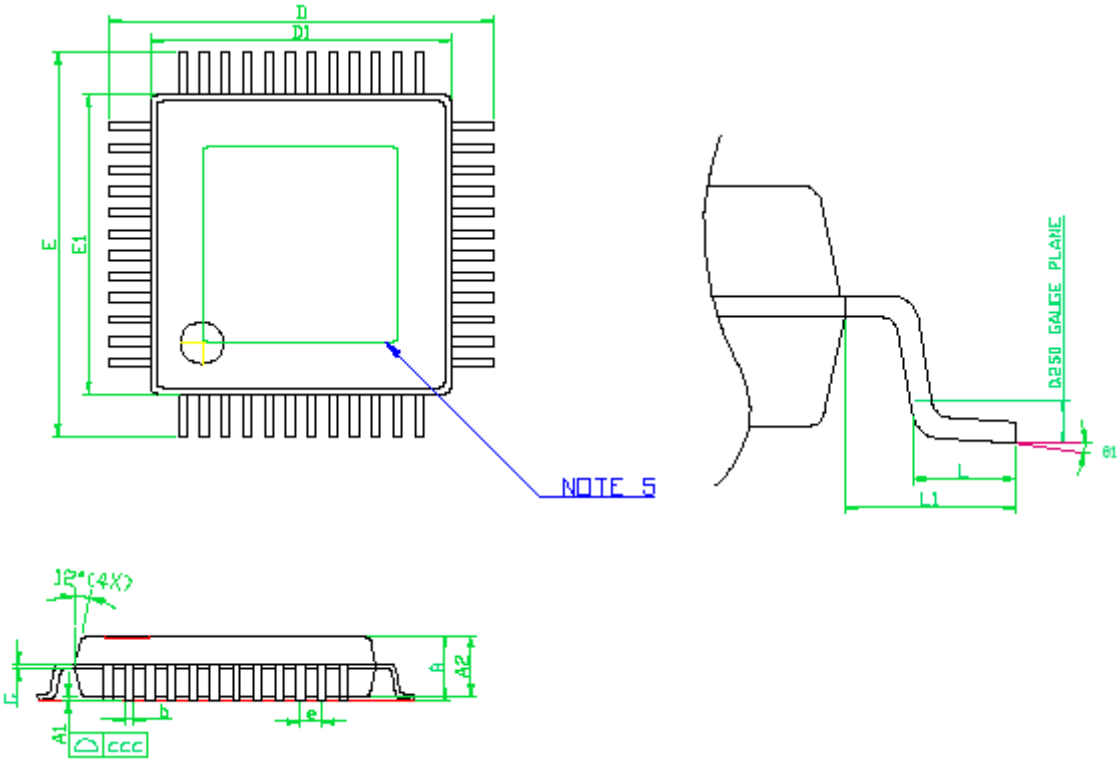


Figure 12. Stereo Class D with Single-Ended Inputs

PACKAGE DIMENSION

TQFP-48-EP



SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	——	1.15	——	——	0.046
A1	0.05	——	0.15	0.002	——	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.006	0.008	0.011
C	0.09	-----	0.20	0.003	----	0.008
D1	6.90	7.00	7.10	0.271	0.275	0.279
D	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.90	7.00	7.10	0.271	0.275	0.279
E	8.80	9.00	9.20	0.346	0.354	0.362
e	——	0.50(TYP)	——	——	0.02(TYP)	——
L	0.45	0.60	0.75	0.018	0.024	0.029
L1	——	1.00(REF)	——	——	0.039(REF)	——
θ1	0°	3.5°	7°	0°	3.5°	7°
ccc	----	----	——	----	----	0.0035

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS
2. DIMENSION L IS MEASURED IN GAUGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. DIE PAD EXPOSURE SIZE IS ACCORDING TO LEAD FRAME DESIGN.
6. FOLLOWED FORM JEDEC MO-136

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